Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2)

Specification Update

December 2003

Notice: The P64H2 may contain design defects or errors known as errata. Characterized errata that may cause the P64H2's behavior to deviate from published specifications are documented in this specification update.

Order Number: 290735-015

Contents

Revision History

Revision	Version	Description	Date
-001	1.0	• Initial Release	February 2002
-002	1.0	• Added Errata # 2 • Added Specification Clarification #1, #2 • Added Documentation Change #1, #2	May 2002
-003	1.0	• Added Specification Clarification #3	July 17, 2002
-004	1.0	• Updated Documentation Change #2 • Added Documentation Change #3, #4	August 2002
-005	1.0	• Added Errata #3 • Added Documentation Change #5	September 2002
-006	1.0	• Documentation Change #6	October 2002
-007	1.0	• Update to Errata #3 • Identification Markings • Documentation Change #7	December 2002
-008	1.0	• Rev 001-007 of this doc has been incorporated in Rev 002 of the P64H2 Datasheet • Specification Clarification #1 • Document Change #1, #2 (incorporated with Rev 002 of P64H2 Datasheet)	January 2003
-009	1.0	• Added Specification Clarification #2	March 2003
-010	1.0	• Added Specification Change #1	April 2003
-011	1.0	• Added Specification Clarification #3	May 2003
-012	1.0	• Added Document Change #3	June 2003
-013	1.0	• Added Specification Clarification #4	July 2003
-014	1.0	• Added Specification Errata #4	August 2003
-015	1.0	• Added Document Change #4, #5	December 2003

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet	290732-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2). Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Bar:	This item is either new or modified from the previous version of the document.

Errata

No.	Stepping	Stepping	Status	ERRATA
	B0	B1		
1	X	X	No Fix	Split Completion Message for Inbound Dword Read has Incorrect Remaining Address Field
2	X	X	No Fix	Hub Interface during Hinted Peer-to-Peer Writes
3	X		Fixed	PCI-X Arbitration
4	X		No Fix	Discard Timer

Specification Changes

No.	SPECIFICATION CHANGES
1	CLK133 Cycle to Cycle Jitter (Tccjitter) Specification

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	Bridge_CNT - Bridge Control Register (D29, D31:F0)
2	Address Parity Checking on DAC
3	Table 83 P64H2 Clock Timings
4	PERR# Implementation

Documentation Changes

No.	DOCUMENTATION CHANGES
1	XOR Chain #3 (HI_16)
2	Revision ID Registers
3	Table 62: VCC5REF Minimum Value
4	Datasheet Document Number Reference
5	I/O APIC Device 30 & 28

Identification Information

Markings

The P64H2 chipset can be identified by the following component markings:

Stepping	QDF#	S-Spec	Top Marking	Notes
B0	N/A	SL675	82870P2	Production
B1	N/A	SL6SU	82870P2	Production

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Errata

1. Split Completion Message for Inbound Dword Read has Incorrect Remaining Address Field

Problem: P64H2 does not set the lower address field to zero for a split completion message in response to DWord read request. This violates section 2.10.6 of PCI-X specification, which states that the lower address field in the Split Completion address should be set to zero.

Implication: Sensitivity to this spec violation would only occur in a P64H2 platform if a read request was sent to a device over the Hub Interface by the P64H2, and the device responded with a master/target abort. Under normal system operation, the MCH and the SIOH devices will not return a master/target abort; therefore, this spec violation will not affect the operation of the P64H2.

Workaround: None.

Status: No fix.

2. Hub Interface Starvation During Hinted Peer-to-Peer Writes

Problem: When continuous hinted peer-to-peer writes occur between PCI segments of the P64H2, a starvation condition may occur, stalling all Hub Interface traffic. The P64H2 does not arbitrate Hub Interface traffic effectively during hinted peer-to-peer writes. Once the hinted peer-to-peer writes complete, Hub Interface traffic can continue.

Workaround: This is a performance related issue that could result in a Hub Interface timeout condition. This issue has only been reproduced in a testing enviornment using synthetic applications under heavy stress loads.

It may be necessary to limit **continuous** hinted peer-to-peer writes through the P64H2; periodic interruptions to the flow of hinted peer-to-peer writes will insure the Hub Interface will not stall.

Status: No fix.

3. PCI-X Arbitration

Problem: When a PCI-X agent requests and is granted the bus but then removes the request without running a cycle, it is possible for the PCI-X arbiter to issue back-to-back grants to other agents without the required 1 clock delay for turn around time, resulting in bus contention.

Implication: Investigation to date shows this erratum may be exposed when an agent asserts its requests, gets the grant, and removes the request after 4 or 5 clocks of sampling the bus idle and active grant without initiating any cycle during this period. Subsequent pending requests can result in the P64H2 asserting GNT# to multiple masters without providing the necessary turn-around clock in-between.

A system that uses an affected stepping of the P64H2 with a PCI-X bus mastering card that exhibits this behavior described, may encounter system hang or blue screen. Data integrity is protected by PCI parity protocol.

Workaround: A BIOS workaround has been implemented to detect the PCI-X device(s) that would exhibit this behavior. Once detected, the BIOS will initialize the bus segment to operate in PCI mode. Refer to the *Intel® P64H2 BIOS Specification Update Rev 1.32*.

Status: Fixed in B1 stepping

4. Discard Timer

Problem: A PCI master makes an upstream read request and abandons this request before any data is returned. Since the card doesn't retry the read, P64H2 is suppose to discard the delayed transaction using a discard timer. In certain timing conditions, the discard timer will not expire and the transaction is not discarded. A PCI master that abandons the read request before any data is returned is not compliant to the PCI 2.2/2.3 Specification.

Implication: A bug may be encountered in a environment when using the P64H2 with a PCI master card with the above non-PCI 2.2/2.3 compliant behavior under certain timing conditions. This could cause a delayed transaction to not be evicted and result in an infinite retry/system hang. This bug was found in a synthetic environment with a test card and there a no known failures with real devcies.

Workaround: None.

Status: No Fix.

Specification Changes

1. CLK133 Cycle to Cycle Jitter (Tccjitter) Specification

In Table 83, under CLK133 Tccjitter Max is 400ps.

Specification Clarifications

1. Bridge_CNT - Bridge Control Register (D29, D31:F0)

In Section 3.2.21, it incorrectly mentions the usage of this register. The two Secondary Buses are not controlled via one single register D31:F0 but are controlled by Bridge Control Registers in D31:F0 and D29:F0 respectively. The register defintion remains the same for both the registers.

2. Address Parity Checking on (Dual Address Cycle) DAC

P64H2 will check the address parity only on AD[31:0] for a DAC. Parity on full 64 bits of the address will be covered by checking the parity on AD[31:0] on the first and the second address phases of DAC.

3. Table 83 P64H2 Clock Timings

Make the following changes to Table 83 -

Symbol	Parameter	Min	Max	Units	Notes
—	Input Clocks				
CLK66 – Hub Interface Input Clock	CLK period	15.0	15.3	ns	1,2
T_{high}	CLK high time	4.95	N/A	ns	3
T_{low}	CLK low time	4.55	N/A	ns	4
T_{rise}	CLK rise time	0.5	2.0	ns	5
T_{fall}	CLK fall time	0.5	2.0	ns	5
—	Rising edge rate	1.0	4.0	V/ns	5
—	Falling edge rate	1.0	4.0	V/ns	5
CLK200 - Hub Interface Input Clock					
T_{period}	Average Period	5.0	5.2	ns	6
T_{rise}	Rise time across 600 mV	300	600	ps	7,8
T_{fall}	Fall time across 600 mV	300	600	ps	7,8
—	Rise/Fall Matching		20%		7,9
—	Cross point at 1 V	0.51	0.76	V	
$T_{ccjitter}$	Cycle to Cycle jitter		200	ps	
—	Duty Cycle	45	55	%	
—	Maximum voltage allowed at input		1.45	V	
—	Minimum voltage allowed at input		-200	mV	
T_{Vring_rise}	Rising edge ringback	0.85		V	
T_{Vring_fall}	Falling edge ring back		0.35	V	
CLK100					
—	Maximum voltage allowed at input		1.45	V	
—	Minimum voltage allowed at input		-200	mV	
CLK133					
—	Maximum voltage allowed at input		1.45	V	

Output Clocks					
CLK100					
T_{period}	Average Period	10.0	10.2	ns	6
T_{rise}	Rise time across 600 mV	300	600	ps	7,8
T_{fall}	Fall time across 600 mV	300	600	ps	7,8
—	Rise/Fall Matching		20%		7,9
—	Cross point at 1 V	0.51	0.76	V	
$T_{ccjitter}$	Cycle to Cycle jitter		200	ps	
—	Duty Cycle	45	55	%	
—	Rising edge ringback	0.85		V	
—	Falling edge ring back		0.35	V	
CLK133					
T_{period}	Average Period	7.5	7.65	ns	6
T_{rise}	Rise time across 600 mV	300	600	ps	7,8
T_{fall}	Fall time across 600 mV	300	600	ps	7,8
—	Rise/Fall Matching		20%		7,9
—	Cross point at 1V	0.51	0.76	V	
$T_{ccjitter}$	Cycle to Cycle jitter		200	ps	
—	Duty Cycle	45	55	%	
—	Rising edge ringback	0.85		V	
—	Falling edge ring back		0.35	V	
CLK33					
T_{period}	CLK period	30.0	N/A	ns	1,2
T_{high}	CLK high time	12.0	N/A	ns	3
T_{low}	CLK low time	12.0	N/A	ns	4
—	Rising edge rate	1.0	4.0	V/ns	5
—	Falling edge rate	1.0	4.0	V/ns	5
T_{rise}	CLK rise time	0.5	2.0	ns	5
T_{fall}	CLK fall time	0.5	2.0	ns	5
APICCLK					
f_{ioap}	Operation Frequency	14.32	33.33	MHz	
T_{high}	High time	12	36	ns	
T_{low}	Low time	12	36	ns	
T_{rise}	Rise time	1.0	5.0	ns	
T_{fall}	Fall time	1.0	5.0	ns	

Notes:

1. Period, jitter, offset and skew measured on rising edge @ 1.5 V for 3.3 V clocks.
2. The average period over any 1 us period of time must be greater than the minimum specified period.
3. T_{high} is measured at 2.4 V for non-host outputs.
4. T_{low} is measured at 0.4 V for all outputs.
5. For 3.3 V clocks T_{rise} and T_{fall} are measured as a transition through the threshold region V_{ol} = 0.4 V and V_{oh} = 2.4 V (1 mA) JEDEC Specification.
6. Measured at crossing point.
7. Measured from V_{ol} = 0.2 V to V_{oh} = 0.8 V.
8. Still simulating to determine [0.2–0.8 V] or [0.3–0.9 V].
9. Determined as a fraction of $2*(T_{rise} - T_{fall}) / (T_{rise} + T_{fall})$.

4. PERR# Implementation

The P64H2 does not escalate a data parity mismatch reported by a PCI device (PERR#) across the P2P bridge while in PCI Mode. The PCI Specification or P2P Bridge Spec does not require PERR# escalation across a P2P bridge.

For certain applications, it may be desirable to generate an SMI or NMI upon PERR# assertion by a PCI device. The device/driver is expected to handle such situations by retrying the transactions or escalating to the OS via device driver. Alternatively, external circuitry can be added to platforms to drive SMI or NMI upon PERR# assertion.

The P64H2 does escalate a data parity mismatch reported by a PCI device (PERR#) across the P2P bridge while in PCI-X Mode.

Documentation Changes

1. XOR Chain #3 (HI_16)

In Section 7.2, Table 87 XOR Chain Table change the second occurance of HI_16 to HI_20.

....
Hi_3
HI_20
HI_6
....

2. Revision ID Registers

In Sections 3.2 (Table 15), 3.2.5, 3.3.1.5 and 3.4.1.5 respectively, make the following changes:

08h	RID	Revision Identification	04h	RO

RID—Revision ID Register (D29,31: F0)

Offset: 08h
Default Value: 04h
Attribute: RO
Size: 8 bits

Bits	Description
7:0	**Revision ID (RID).** This field indicates the stepping of the Intel® P64H2: 03h = B0 Stepping 04h = B1 stepping

RID—Revision ID Register (Device 31)

Offset:	08h	Attribute:	RO
Default Value:	04h	Size:	8 bits

Indicates the revision of the hot plug controller.

Bits	Description
7:0	**Revision ID (RID).** This filed indicates the stepping of the Intel® P64H2. 03h = B0 Stepping 04h = B1 Stepping

RID—Revision ID Register (D28,30: F0)

Offset:	08h	Attribute:	RO
Default Value:	04h	Size:	8 bits

Bits	Description
7:0	**Revision ID (RID).** Indicates the step of the I/OxAPIC in the Intel® P64H2. 03h = B0 Stepping 04h = B1 Stepping

3. Table 62: VCC5REF Minimum Voltage

In Table 62 P64H2 DC Voltage Characteristics, change the minimum value for VCC5REF to 3.0V.

Table 62 Intel® P64H2 DC Voltage Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VCC1.8	P64H2 Core and HI2.0 I/O supply	1.71	1.8	1.89	V
VCC1.8 Transient	VCC1.8 Transient Tolerance			± 5%	V
VCC3.3	PCI Bus Interface	3.135	3.3	3.465	V
VCC3.3 Transient	VCC3.3 Transient Tolerance	Y		± 5%	V
VCC5REF	5V Reference for PCI Bus	3.0	5.0	5.25	V
VCC1.8dI/dt	P64H2 Core and HI2.0 I/O			2.1	A/ns
VCC3.3dI/dt	Transient Core Tolerance			1.32	A/ns
P_{TDP}	Thermal Design Power			4.6	W

4. Datasheet Document Number Reference

In this Spec Update, under the Affected Documents/Related Documents section, the correct document number for the Datasheet is 290732-002.

5. I/O APIC Device 30 & 28

In Sections 1.2, 3, 3.4, and 4.6, device 30 & 28 are incorrectly referenced. It should state that “the interrupts from PCI bus A is connected to the interrupt controller on device ~~28~~ 30 and the interrupts on PCI bus B is connected to the interrupt controller on device ~~30~~ 28”.

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